FPGA BLOCKS WITH ADJUSTABLE POROSITY PASS THRU

ABSTRACT OF THE DISCLOSURE

A field programmable gate array is described for use in a semiconductor chip such as a VLSI chip. The array is provided with variable wire-through porosity to allow for optimum chip-level routing through the array. This is achieved by dividing the array into blocks which can be individually assessed for required porosity. Then blocks that have been prefabricated with differing porosities are placed in the macro to optimize local chip level routing. The routing of wires is determined by developing a chip floor plan to include early timing allocation and a proposed placement of the array. The floor plan is then overlaid with critical logical wiring nets. From this, an initial selection of blocks is made based on proposed wiring density, and the macro is assembled with the blocks strategically placed therein. The procedure is likewise applicable to other types of densely obstructed cores embedded with a chip.